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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/604,381	07/16/2003	Pao-Ching Tseng	MTKP0048USA	1380
27765	7590	04/18/2006	EXAMINER	
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION P.O. BOX 506 MERRIFIELD, VA 22116			PATEL, KAUSHIKKUMAR M	
			ART UNIT	PAPER NUMBER
			2188	

DATE MAILED: 04/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/604,381	Applicant(s) TSENG ET AL.	
	Examiner Kaushikkumar Patel	Art Unit 2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 February 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-8 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-8 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Amendment

1. This Office Action is in response to applicant's communication files February 9, 2006 in response to PTO Office Action mailed November 16, 2005. The Applicant's remarks and amendments to the claims were considered with the results that follow.
2. In response to the last Office Action, no claims have been amended. Claims 6-8 have been added. As a result, claims 1-8 remain pending in this application.

Response to Arguments

3. Applicant's arguments with respect to claims 1-5 have been considered but are moot in view of the new grounds of the rejection.

Claim Objections

4. Claim 2 is objected to because of the following informalities:

Acronym such as MCS in claim 2 should not be used to abbreviate key terms or phrases until they are explicitly defined previously within the claim or in a claim to which it depends. An acceptable correction would be for example in claim 2, Microcontroller series (MCS).

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Zhou et al. (5,913,924) (Zhou herein after).

As per claim 1, Zhou teaches a method for accessing a memory having a storage space larger than the addressing capacity of a microprocessor (abstract, figs. 4-5), the memory comprising a plurality of memory banks (fig. 1), the microprocessor comprising a stack (column 6, line 66), an interrupt processing unit, and a memory bank selector for selecting the memory banks (column 6, lines 49-55), the method comprising:

(a) storing an interrupt service routine in one of the memory banks (column 6, lines 50-52);

(b) when an interrupt occurs, pushing a current program counter address onto the stack by the interrupt processing unit, pushing a bank number of the current memory bank onto the stack, and setting the memory bank selector to the bank number of the memory bank storing the interrupt service routine (column 6, lines 65-67, column 7, lines 10-37);

(c) switching the microprocessor to the memory bank storing the interrupt service routine to execute the interrupt service routine (column 7, lines 25-35, only memory

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bank 370 A stores interrupt service routine, and during program execution in bank 370B, after interrupt switches to bank 370A for interrupt service routine);

(d) after interrupt service routine finishes execution, popping the bank number of the memory bank stored in the step (b) from the stack by the interrupt processor unit, restoring the popped bank number to the memory bank selector, and popping program counter address stored in the stack in step (b) from the stack (column 7, lines 6-9, lines 41-59);

(e) switching the microprocessor back to the memory bank corresponding to the bank number stored in the memory bank selector to continue executing the program interrupted in step (b) (column 7, lines 55-59).

As per claim 2, Zhou teaches microprocessor is Microcontroller series processor (column 4, line 39).

As per claim 3, Zhou teaches common area in each memory bank (fig. 3, items 375A and 375B).

As per claim 4, Zhou teaches memory banks storing interrupt service routine in only in one memory bank separate from bank selection routine (column 7, lines 60-67).

As per claim 5, Zhou teaches single chip microprocessor (fig.3, item 310).

Claims 6-8 are also rejected under same rationales as applied to claims 1-5 above, as Zhou teaches a device (computer system, see abstract), with microprocessor and plurality of memory banks as applied to claims 1-5 above.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Bjerger et al. (5,655,099) teaches bank switching access program instructions stored in one memory bank.

Kaneko (5,146,581) teaches multiple memory banks storing interrupt service routines for bank switching.

Ma et al. (US 6,691,219) teaches extending memory address range and interrupt processing in multi-bank memories.

Takiguchi et al. (5,557,766) teaches bank-structured memories capable of handling multiple interrupts.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kaushikkumar Patel whose telephone number is 571-272-5536. The examiner can normally be reached on 8.00 am - 4.30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kaushikkumar Patel
Examiner
Art Unit 2188

kmp

Mano Padmanabhan
4/14/06

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER